Comparing Sandy Bridge vs. Ivy Bridge processors for HPC applications

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As new server technologies become available, each generation is touted as being better, faster, more efficient, and laden with new features. For an HPC user, the question is "how much better?", "how much faster?" and especially, "how much does it benefit my specific application?"

For nearly 30 years, the National Center for Supercomputing Applications (NCSA) has been a leading site for some of the world's most advanced computing and data systems. NCSA's Private Sector Program (PSP) is also the largest industry engagement effort at an HPC center in America, providing computing, data, and other resources to help companies leverage supercomputing to solve the most challenging science and engineering problems.

This blog presents some of the work conducted by NCSA's PSP to measure and analyze the performance benefits of the new Intel Xeon E5-2600 v2 processors (code-named Ivy Bridge) over the previous generation E5-2600 series (code-named Sandy Bridge). The focus here is on various HPC applications widely-used by researchers and designers in the manufacturing sector. A mix of commercial and open source applications like ANSYS Fluent, LS-DYNA, Simulia Abaqus, MUMPS, and LAMMPS were selected for this investigation. High-Performance Linpack (HPL) benchmark results are also presented.

The main difference between the two processor generations under study is the shrinking of process technology from 32nm to 22nm. This allows fitting more transistors on the chip, higher clock rates, and better power management. For example, running the SPEC power benchmark with 100% load on Dell Power Edge R720 with Ivy Bridge (IVB) Intel Xeon E5-2660 v2 showed 25% lower peak CPU power consumption compared to HUAWEI Tecal RH2288 V2 server with Sandy Bridge (SB) Xeon E5 2660. A 2.0 GHz SB processor runs at max TDP of 60W whereas a 2.0 GHz IVB processor runs at max TDP 50W. Also for processors with maximum TDP 150W the clock speed of IVB (3.4 GHz) is higher than that of SB processors (3.1 GHz). It is essential for users to understand the power and frequency differences between the two generations before selecting a processor for their application. Both processors have an integrated memory controller that supports four DDR3 channels. SB processors support memory speeds up to 1600 MT/s, whereas IVB support memory speeds up to 1866 MT/s.

When selecting a CPU for your application it is important to consider factors like power consumption, usable bandwidth (for applications on multiple nodes) along with the clock speed and the number of cores.

Table 1 gives more information about the application and the hardware configuration used for the tests.

Table 1: Hardware Configuration & Application details

	16 core Sandy Bridge	20 core Ivy Bridge	24 core Ivy Bridge
Processor	2 x Intel Xeon E5 2670 @ 2.6GHz (8-core)	2 x Intel Xeon E5 2680 v2 @ 2.8GHz (10-core)	2 x Intel Xeon E5 2697 v2 @ 2.7GHz (12-core)
Memory	128GB 1600MHz	256GB 1866MHz*	256GB 1600MHz
Operating System	RHEL 6.4		
File System	IBM GPFS, 700TB disk, 8 Storage Servers (PowerEdge R710) each 192GB RAM and 1.5TB of I/O cache		
Applications/ Benchmarks	ANSYS Fluent 14.5		
	LS-DYNA 6.1.1.790306		
	LAMMPS 12		
	MUMPS 4.10.0	(not used)	MUMPS 4.10.0
	Simulia Abaqus E6 6.12	(not used)	Simulia Abaqus E6 6.12
	Simulia Abaqus S4B 6.12	(not used)	Simulia Abaqus S4B 6.12
	HPL	(not used)	HPL

* 1866MHz unless otherwise noted

Figure 1 shows the performance gain with 12-core IVB processors over the 8-core SB processors for various applications. For each application, the baseline is the Sandy Bridge system. Tests were conducted on a single node with 2 * Intel Xeon E5 2670 (8-core) SB processor and 2 * Intel Xeon 2697 v2 (12-core) IVB processors as noted in Table 1.

Figure 1: Performance gain with Ivy Bridge (12-core) vs. Sandy Bridge (8-core)

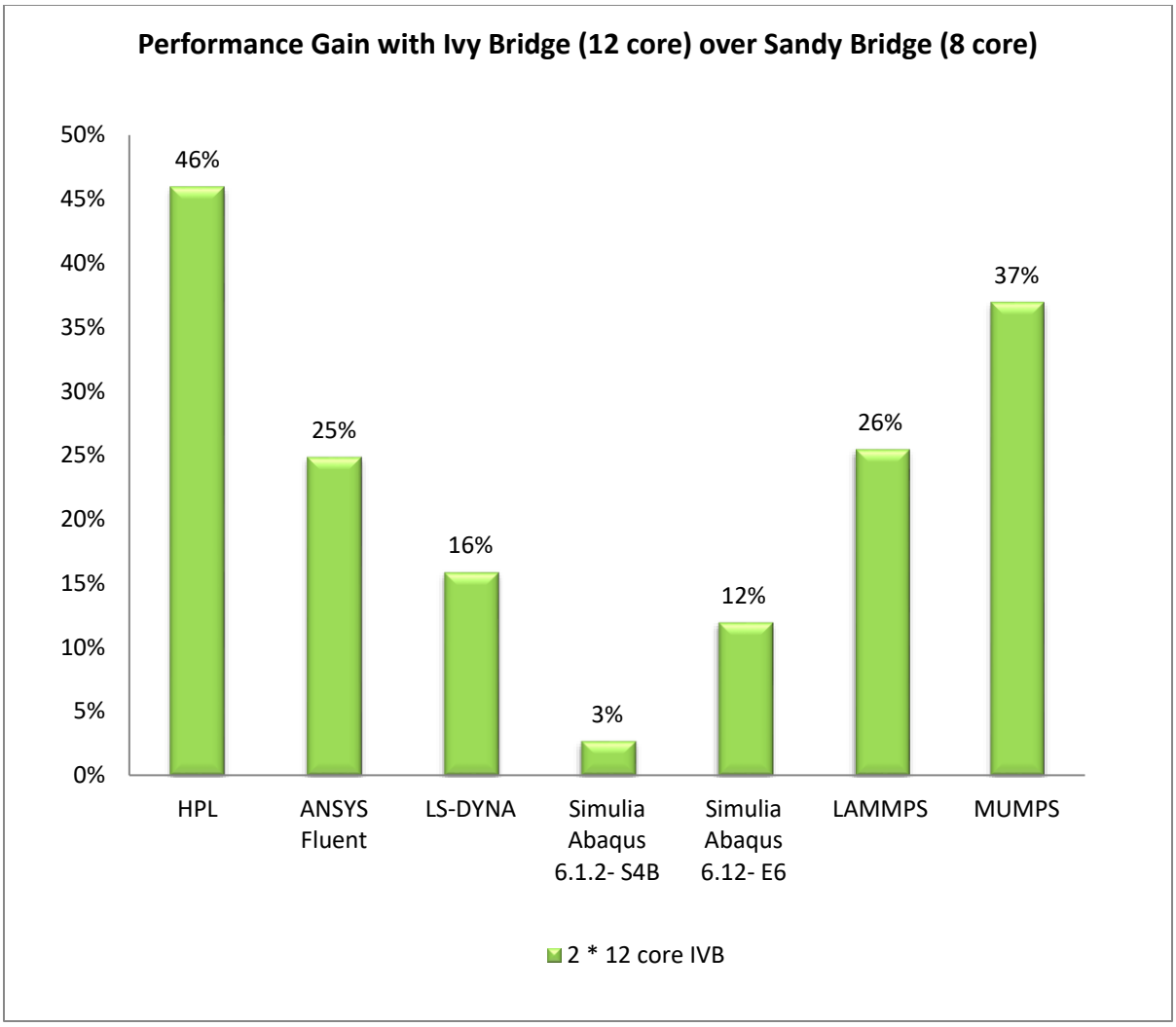
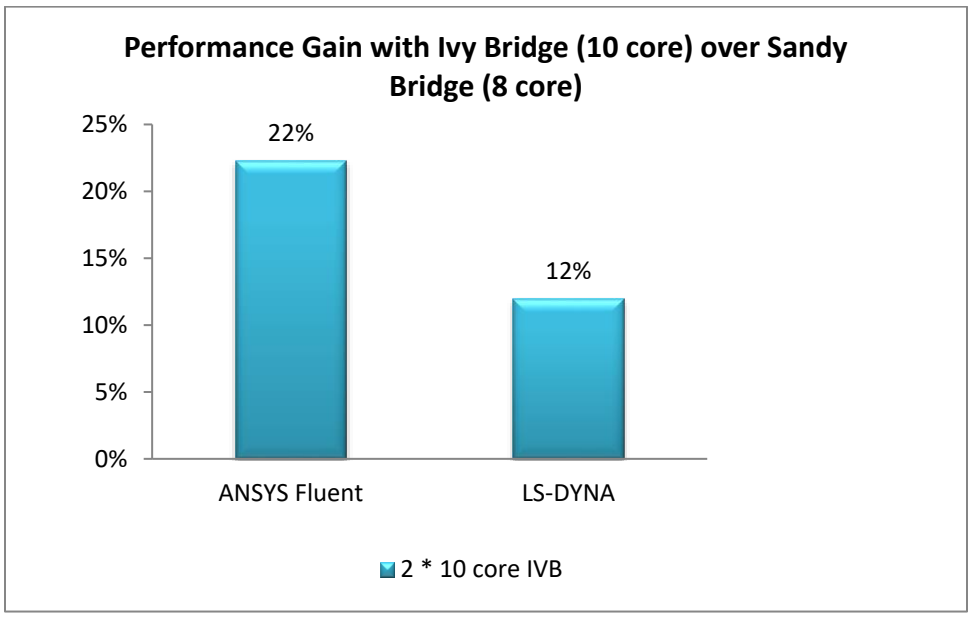


Figure 1 compares the performance of HPL. HPL solves a random dense linear system in double-precision arithmetic on distributed-memory systems. The problem size (N) used for the 12core IVB system was ~81% of the total memory size. Since HPL is a CPU-intensive benchmark, higher performance is expected with higher clock frequencies and more cores. BIOS Turbo mode was enabled for this test. The performance achieved with the IVB processor was ~1.5 times more than that measured with SB. Note that the performance gain with IVB measured by this synthetic benchmark is much greater than that measured for actual applications. This truly emphasizes the value of the detailed application benchmarking studies conducted by NCSA! Using just micro-benchmark and synthetic benchmark data to evaluate systems doesn't always translate into gains for real-world use cases.

Figure 1 shows 25% performance gain with IVB on ANSYS Fluent, a computational fluid dynamics application. The benchmark problem used was a turbulent reacting flow case with large eddy simulation. The case has around 4 million unstructured hexahedral cells. The BIOS Turbo mode was disabled for the test. Figure 2 compares the performance of the 10 core IVB to the 8 core SB processor, which shows a 22% performance gain for the IVB processors against the SB processors. The 12-core IVB processor offers slightly better performance than the 10-core IVB model, which is expected due to the increase in number of cores. Note that this test disabled Turbo and hence we're

comparing the rated base CPU frequency. In cases where Turbo is enabled, both IVB and SB processors can operate at higher clock rates and that should be taken into account when comparing results.

Figure 2: Performance gain with Ivy Bridge (10-core) vs. Sandy Bridge (8-core) for ANSYS Fluent and LS-DYNA



LS-DYNA is a general-purpose finite element program from LSTC capable of simulating complex real-world structural mechanics problems. The “Dodge Neon Refined Revised” benchmark is a higher resolution mesh of the standard "Neon" benchmark, and features approximately 5M DOFs. The BIOS Turbo mode was enabled for the test. Here the IVB processors performed 12-16% better compared to the SB processors (as shown in Figure 1 and 2). It will come as little surprise those familiar with LS-DYNA that this observed performance increase tracks linearly with the 16% memory bandwidth increase of IVB platform over the SB platform, proving that application performance is tied to much more than just the sheer number of CPU cores or clock frequency.

Dassault Systèmes’ Abaqus offers solutions to engineering problems covering a vast spectrum of industrial applications. Abaqus/Standard applications include linear statics, nonlinear statics, and natural frequency extraction. The S4B (5M DOF direct solver version) benchmark is a mildly nonlinear static analysis that simulates bolting a cylinder head onto an engine block. It is a more compute intensive benchmark with a high degree of floating point operations per iteration. These types of models scale better than communication-bound benchmarks, like the Abaqus E6 dataset, where more time is utilized in communication of messages versus time spent in the solver.

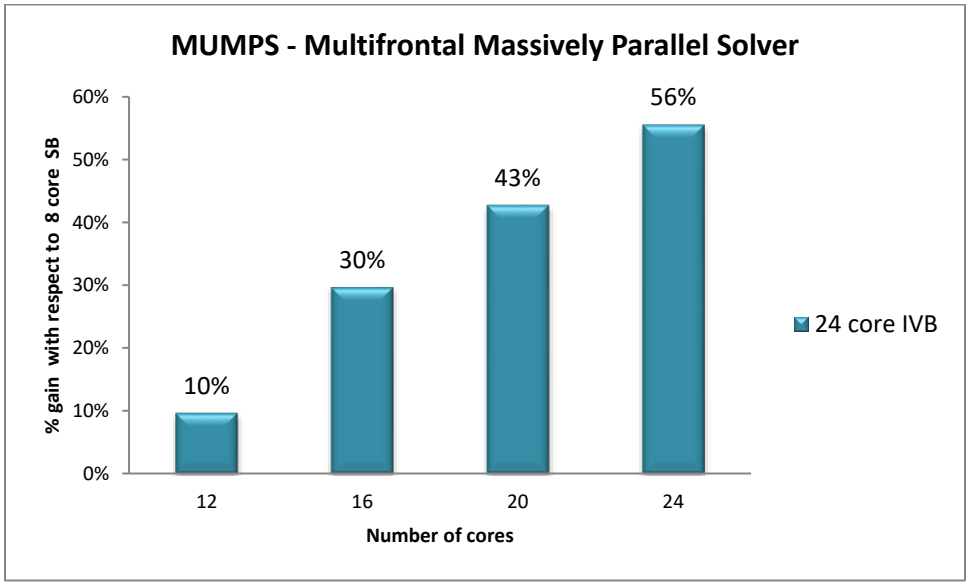
Abaqus/Explicit benchmarks focus on nonlinear, transient, dynamic analysis of solids and structures using explicit time integration. The E6 (concentric spheres with 23,291 increments, 244,124 elements) benchmark consists of a large number of concentric spheres with clearance between each sphere. Abaqus/Explicit E6 model is more communications intensive than Abaqus/Standard, with large systems of equations passing information to one another as they are being solved.

Turbo mode was enabled for both the Abaqus benchmarks. The large arrays of equation solvers and datasets used in the simulation also require a large, fast memory system. For better performance with all applications, it is recommended to install enough memory so the job resides completely in physical memory to minimize I/O swapping to a local or network file system. The results show ~3% and 12% improvement with IVB 24c for the S4B and E6 benchmarks respectively. Test results were gathered using 1600 MHz RAM in both systems. Performance for IVB expected to be 5-10% higher with 1866 MHz RAM.

LAMMPS (Large-scale Atomic/Molecular Massively Parallel Simulator) is an open source classical molecular dynamics simulator designed to run efficiently on parallel machines. The EAM metallic solid benchmark with problem size of 32000 atoms was used here. The BIOS Turbo mode was enabled for the SB processors. The results in Figure 1 show a significant improvement of 26% with the IVB 12 core system. This is expected performance as LAMMPS runs efficiently in parallel using message-passing techniques and scales well with additional number of cores. Also enabling the BIOS Turbo mode option for Ivy Bridge processors did not significantly impact the performance most likely because system is already running close to TDP (Thermal Design Power).

MUMPS (Multifrontal Massively Parallel sparse direct Solver) is a software application for large sparse systems of linear algebraic equations on distributed memory parallel computers. The number of equations solved (norm of the matrix) was N = 1,522,431 and the number of nonzero values used was NNZ = 63639153. BIOS Turbo mode was enabled for the tests. The results were gathered using 1600 MHz RAM in both 8-core SB and 12-core IVB systems. The benchmark measured a 37% performance improvement with 24 cores of IVB over 16 cores of SB. This is primarily due to the increase in number of cores. Breaking this down further, Figure 3 shows the results of scaling within the server. The horizontal X-axis shows the number of cores used for the 24-core IVB system and the Y-axis shows the performance gain achieved compared to 8 cores of the SB processor. As the number of cores increase the problem gets solved faster.

Figure 3: MUMPS - Multifrontal Massively Parallel Solver



Conclusion

NCSA's testing results show that the Ivy Bridge processors provide better performance compared to the Sandy-Bridge for all the applications. The actual improvement depends on the application and its characteristics. The cost/benefit analysis of upgrading to IVB processors should be done based on a particular application workload, and not just based on number cores or higher clock rates. Still, the work conducted by NCSA gives users insights into the performance gains they can expect for these widely-used applications.

Dell and NCSA continue to work together to investigate new HPC technologies and provide clear information to users from industry, with the shared goal of helping this community improve the performance of its applications and make informed, data-driven decisions about its HPC solutions.

If you're interested in leveraging the computing and expertise resources available through NCSA's Private Sector Program, contact Evan Burness at eburness@ncsa.illinois.edu.