DELL Technologies

Statement of Volatility – Dell PowerEdge XR12

Dell PowerEdge XR12 contains both volatile and non-volatile (NV) components. Volatile components lose their data immediately upon removal of power from the component. Non-volatile components continue to retain their data even after the power has been removed from the component. Components chosen as user-definable configuration options (those not soldered to the motherboard) are not included in the Statement of Volatility. Configuration option information (pertinent to options such as microprocessors, remote access controllers, and storage controllers) is available by component separately. The following NV components are present in the PowerEdge XR12 server.

Item	Non-Volatile or Volatile	Quantity	Reference Designator	Size	Type (e.g. Flash PROM, EEPROM)	Can user programs or operating system write data to it during normal operation?	Purpose? (e.g. boot code)	How is data input to this memory?	How is this memory write protected?	How is the memory cleared?
Planar										
PCH Internal CMOS RAM	Non-Volatile	1	U_PCH1	256 Bytes	Battery-backed CMOS RAM	No	Real-time clock and BIOS configuration settings	BIOS	N/A – BIOS only control	1) Set NVRAM_CLR jumper to clear BIOS configuration settings at boot and reboot system. 2) Power off the system, remove coin cell battery for 30 seconds, replace battery and then power back on. 3) Restore default configuration in F2 system setup menu.
BIOS SPI Flash	Non-Volatile	1	U16	32 MB	SPI Flash	No	Boot code, system configuration information, UEFI environment, ME	SPI interface via PCH	Software write protected	Not possible with any utilities or applications and system is not functional if corrupted or removed.

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BIOS Data SPI Flash	Non-Volatile	1	U19	4 MB	SPI Flash	No	4MB Data SPI ROM storage BIOS setting.	SPI interface via PCH	Software write protected	Not possible with any utilities or applications and the system is not functional if BIOS SPI is corrupted or removed.
iDRAC SPI Flash	Non-Volatile	1	U40	4 MB	SPI Flash	No	iDRAC Uboot (boot loader), server management persistent store (i.e. iDRAC boot variables), and virtual planar FRU	SPI interface via iDRAC	Embedded iDRAC subsystem firmware actively controls sub area based write protection as needed.	The user cannot clear memory completely. However, user data, lifecycle log and archive, SEL, and firmware image repository can be cleared using Delete Configuration and Retire System, which can be accessed through the Lifecycle Controller interface.
BMC EMMC	Non-Volatile	1	U38	8 GB	eMMC NAND Flash	No	Operational iDRAC FW, Lifecycle Controller (LC) USC partition, LC service diags, LC OS drivers, USC firmware, IDRAC MAC Address, and	NAND Flash interface via iDRAC	Embedded FW write protected	The user cannot clear memory completely. However, user data, lifecycle log and archive, SEL, and firmware image repository can be cleared using Delete Configuration and Retire System, which can be

Item	Non-Volatile or Volatile	Quantity	Reference Designator	Size	Type (e.g. Flash PROM, EEPROM)	Can user programs or operating system write data to it during normal operation?	Purpose? (e.g. boot code)	How is data input to this memory?	How is this memory write protected?	How is the memory cleared?
							EPPID, rac log, System Event Log, lifecycle log cache			accessed through the Lifecycle Controller interface.
iDRAC DDR4	Volatile	1	U31	8Gb	RAM	Yes	iDRAC RAM	iDRAC firmware	Not write-protected	Remove AC
System CPLD RAM	Volatile	1	U_CPLD1	240 kb	RAM	No	Not utilized	Not utilized	Not accessible	Not accessible
System CPLD Flash	Non-Volatile	1	U_CPLD1	256 kb	FLASH	No	Power on System Firmware	Firmware update	BIOS Security Protocols	Not user clearable
System Memory: RDIMM and LRDIMM	Volatile	Up to 8	CPU1: A1~8	Up to 128GB per DIMM	RAM	Yes	System OS RAM	System OS	OS Control	Reboot or power down system
System Memory: BPS (Memory Mode)	Volatile	Up to 4	CPU1: A5/A6/A7/A8	Up to 128GB per DIMM	BPS	Yes	System OS RAM	System OS	OS Control	OS Control/System BIOS
System Memory: BPS (App Direct Mode)	Non-Volatile	Up to 4	CPU1: A5/A6/A7/A8	Up to 128GB per DIMM	Flash - BPS	No	Data Integrity - Storage	User can read/write date from/to BPS during normal operation	Normal operation: Data is protected because BPS is non-volatile media in this mode.	Using BIOS menu option, select "Persistent Memory" -> Sanitize DIMM

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									AC loss: ADR is triggered to flash Write Pending Queue (WPQ) to BPS media.	
CPU Vcore and VSA Regulators	Non-Volatile	1	PABU1	16KB	OTP (one time programmable)	No	Operational parameters	Once values are loaded into register space a cmd writes to nvm.	There are passwords for different sections of the register space	The user cannot clear memory.
Memory VDDQ Regulators	Non-Volatile	1	PAEU1	16KB	OTP (one time programmable)	No	Operational parameters	Once values are loaded into register space a cmd writes to nvm.	There are passwords for different sections of the register space	The user cannot clear memory.
LOM SPI Flash	Non-Volatile	1	U_LOM_NVRAM	128 Mb	SPI Flash EEPROM	Yes	Firmware, configuration data	Firmware and some configuration data flashed via Dell Update Package (DUP); some configuration	Reserving write protection function for HW design.	User cannot clear the memory.

Item	Non-Volatile or Volatile	Quantity	Reference Designator	Size	Type (e.g. Flash PROM, EEPROM)	Can user programs or operating system write data to it during normal operation?	Purpose? (e.g. boot code)	How is data input to this memory?	How is this memory write protected?	How is the memory cleared?
								data is programmed during manufacturing; end user configuration data is written via UEFI HII		
6x2.5" Universal SAS/SATA /PCIe Backplane										
SEP internal flash	Non-Volatile	1	U47	Flash: 512KB Data SRAM : 256KB Battery Powered Storage SRAM : 64B	Integrated Flash + Data SRAM + Battery Powered Storage SRAM	No	Firmware + FRU	I2C interface via iDRAC	Program write protect bit	Not user clearable
H755 Adapter PERC (Internal Controller)										
SDRAM	Volatile	9	U1077~U1085	8GB	SDRAM	No	Cache for HDD I/O	ROC writes to this memory - using it as	no write protected. Not visible to Host Processor	Cache can be cleared by powering off the card

Item	Non-Volatile or Volatile	Quantity	Reference Designator	Size	Type (e.g. Flash PROM, EEPROM)	Can user programs or operating system write data to it during normal operation?	Purpose? (e.g. boot code)	How is data input to this memory?	How is this memory write protected?	How is the memory cleared?
								cache for data IO to HDDs		
NV Flash	Non-volatile	1	U1100	512Gb	SPI Flash	No	Card firmware	Pre-programmed before assembly. Can be updated using Dell/LSI tools	no write protected. Not visible to Host Processor	User cannot clear the memory.
BMU	Non-Volatile	1	U1126	180KB	Integrated Flash + EEPROM	No	Battery Management Control	ROC may program data during FW and during boot during battery detection	Not write protected Not visible to host CPU	User cannot clear this memory
SPI Flash	Non-Volatile	1	U1086	128Mb	SPI Flash	No	Holds cache data during power loss	FPGA backs up DDR data to this device in case of a power failure	no write protected. Not visible to Host Processor	Flash can be cleared by powering up the card and allowing the controller to flush the contents to VDs. If the VDs are no longer available, cache can be cleared by going into controller BIOS and

Item	Non-Volatile or Volatile	Quantity	Reference Designator	Size	Type (e.g. Flash PROM, EEPROM)	Can user programs or operating system write data to it during normal operation?	Purpose? (e.g. boot code)	How is data input to this memory?	How is this memory write protected?	How is the memory cleared?
										selecting Discard Preserved Cache.
NVSRAM	Non-volatile	1	U1087	128KB	NVSRAM	No	Configuration data	ROC writes configuration data to NVSRAM	no write protected. Not visible to Host Processor	User cannot clear the memory.
FRU	Non-volatile	1	U1019	2Kb	EEPROM	No	Card manufacturing information	Programmed at ICT during production.	no write protected	User cannot clear the memory.
SPD	Non-volatile	1	U22	2Kb	EEPROM	No	Memory configuration data	Pre-programmed before assembly	no write protected. Not visible to Host Processor	User cannot clear the memory.
CPLD	Non-volatile	1	U1088	64kb	Flash	No	Power sequencing and Cache Offload	ROC may program data during FW update	Not write protected Not visible to host CPU	User cannot clear this memory
MCU (Cordoba)	Non-volatile	1	U41	8KB	EEPROM	No	PCIe Bifurcation information to system iDRAC	BMC may program data if there is an updated version packaged with iDRAC	Not write protected Not visible to host CPU	User cannot clear this memory
H345 Adapter PERC (Internal Controller)										

Item	Non-Volatile or Volatile	Quantity	Reference Designator	Size	Type (e.g. Flash PROM, EEPROM)	Can user programs or operating system write data to it during normal operation?	Purpose? (e.g. boot code)	How is data input to this memory?	How is this memory write protected?	How is the memory cleared?
SPI Flash	Non-Volatile	1	U2	256Mb	SPI Flash	No	Holds cache data during power loss	FPGA backs up DDR data to this device in case of a power failure	no write protected. Not visible to Host Processor	Flash can be cleared by powering up the card and allowing the controller to flush the contents to VDs. If the VDs are no longer available, cache can be cleared by going into controller BIOS and selecting Discard Preserved Cache.
NVSRAM	Non-volatile	1	U5	128KB	NVSRAM	No	Configuration data	ROC writes configuration data to NVSRAM	no write protected. Not visible to Host Processor	User cannot clear the memory.
CPLD	Non-volatile	1	U7	24Kb	Flash	No	Power sequencing and Cache Offload	ROC may program data during FW update	Not write protected Not visible to host CPU	User cannot clear this memory
FRU	Non-volatile	1	U8	64Kb	EEPROM	No	Card manufacturing information	Programmed at ICT during production.	no write protected	User cannot clear the memory.
RMC	Non-volatile	1	U9	64Kb	EEPROM	NO – Only controlled by on-board controller. No	Stores log information.	On-board controller writes to	It is not write protected.	Controller clears the memory.

Item	Non-Volatile or Volatile	Quantity	Reference Designator	Size	Type (e.g. Flash PROM, EEPROM)	Can user programs or operating system write data to it during normal operation?	Purpose? (e.g. boot code)	How is data input to this memory?	How is this memory write protected?	How is the memory cleared?
						way for users or programs to write to it.		EEPROM via I2C interface.		
H840 Adapter PERC (External Controller)										
SDRAM	Volatile	9	U1077~U1085	8GB	SDRAM	No	Cache for HDD I/O	ROC writes to this memory - using it as cache for data IO to HDDs	no write protected. Not visible to Host Processor	Cache can be cleared by powering off the card
NV Flash	Non-volatile	1	U1100	64Gb	SPI Flash	No	Card firmware	Pre-programmed before assembly. Can be updated using Dell/LSI tools	no write protected. Not visible to Host Processor	User cannot clear the memory.
BMU	Non-Volatile	1	U1090	180KB	Integrated Flash+EEPROM	No	Battery Management Control	ROC may program data during FW and during boot during battery detection	Not write protected Not visible to host CPU	User cannot clear this memory

Item	Non-Volatile or Volatile	Quantity	Reference Designator	Size	Type (e.g. Flash PROM, EEPROM)	Can user programs or operating system write data to it during normal operation?	Purpose? (e.g. boot code)	How is data input to this memory?	How is this memory write protected?	How is the memory cleared?
SPI Flash	Non-volatile	1	U1098	128Mb	SPI Flash	No	Holds cache data during power loss	FPGA backs up DDR data to this device in case of a power failure	no write protected. Not visible to Host Processor	Flash can be cleared by powering up the card and allowing the controller to flush the contents to VDs. If the VDs are no longer available, cache can be cleared by going into controller BIOS and selecting Discard Preserved Cache.
NVSRAM	Non-volatile	1	U1087	128KB	NVSRAM	No	Configuration data	ROC writes configuration data to NVSRAM	no write protected. Not visible to Host Processor	User cannot clear the memory.
FRU	Non-volatile	1	U1019	2Kb	EEPROM	No	Card manufacturing information	Programmed at ICT during production.	no write protected	User cannot clear the memory.
SPD	Non-volatile	1	U22	2Kb	EEPROM	No	Memory configuration data	Pre-programmed before assembly	no write protected. Not visible to Host Processor	User cannot clear the memory.
CPLD	Non-volatile	1	U1088	64kb	Flash	No	Power sequencing and Cache Offload	ROC may program data during FW update	Not write protected Not visible to host CPU	User cannot clear this memory

Item	Non-Volatile or Volatile	Quantity	Reference Designator	Size	Type (e.g. Flash PROM, EEPROM)	Can user programs or operating system write data to it during normal operation?	Purpose? (e.g. boot code)	How is data input to this memory?	How is this memory write protected?	How is the memory cleared?
HBA355i (Internal Controller)										
SPI Flash	Non-Volatile	1	U2	128Mb	SPI Flash	No	Card firmware	Pre-programmed before assembly. Can be updated using Dell/LSI tools	Not write protected. Not visible to Host Processor	User cannot clear the memory.
FRU	Non-volatile	1	U5	2Kb	EEPROM	No	Card manufacturing information	Programmed at ICT during production.	Not write protected	User cannot clear the memory.
CPLD	Non-volatile	1	U23	24kb	Flash	No	Power sequencing and Cache Offload	Controller may program data during FW update	Not write protected Not visible to host CPU	User cannot clear this memory
MCU (Cordoba)	Non-volatile	1	U41	8kB	EEPROM	No	PCIe Bifurcation information to system iDRAC	BMC may program data if there is an updated version packaged with iDRAC	Not write protected Not visible to host CPU	User cannot clear this memory
HBA355E (External Controller)										

Item	Non-Volatile or Volatile	Quantity	Reference Designator	Size	Type (e.g. Flash PROM, EEPROM)	Can user programs or operating system write data to it during normal operation?	Purpose? (e.g. boot code)	How is data input to this memory?	How is this memory write protected?	How is the memory cleared?
SPI Flash	Non-Volatile	1	U2	128Mb	SPI Flash	No	Card firmware	Pre-programmed before assembly. Can be updated using Dell/LSI tools	Not write protected. Not visible to Host Processor	User cannot clear the memory.
FRU	Non-volatile	1	U5	2Kb	EEPROM	No	Card manufacturing information	Programmed at ICT during production.	Not write protected	User cannot clear the memory.
CPLD	Non-volatile	1	U23	24kb	Flash	No	Power sequencing and Cache Offload	Controller may program data during FW update	Not write protected Not visible to host CPU	User cannot clear this memory
Status LED Control Panel										
Microcontroller	Non-Volatile	1	U_TINY	8KB	Flash	No	Driving Health and Status LED	I2C via iDRAC	Hardware strapping	User cannot clear the memory.
TPM										
Trusted Platform Module (TPM)	Non-Volatile	1	U2	128 Bytes	EEPROM	Yes	Storage of encryption keys	Using TPM Enabled operating systems	SW write protected	F2 Setup option
Power Button Control Panel										

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SPI Flash	Non-Volatile	1	U2	32 Mb	SPI Flash	No	EasyRestore functionality contains Service Tag, Copy of SEL logs	SPI interface from iDRAC to Right Cntl Panel	Embedded iDRAC subsystem firmware actively controls sub area based write protection as needed.	The user cannot clear memory.
BOSS-S1										
SPI Flash	Non-Volatile	1	U17	1MB	FLASH	No	Boot code, FW	Pre-programmed before assembly; can be updated using Dell tools	Not write protected. Not visible to host processor	Cannot be cleared by user
FRU	Non-Volatile	1	UDFN	2KB	EEPROM	No	Card manufacturing information	Programmed during board build	Not write protected	Cannot be cleared by user
PSU										
DELTA PSU										
Primary MCU	Non-volatile	1	IC805	64KB	Internal Flash	No	Boot code, FW	The data is flash via Dell Update Package (DUP)	SW write protected	Before firmware update, the memory will be cleared.

Item	Non-Volatile or Volatile	Quantity	Reference Designator	Size	Type (e.g. Flash PROM, EEPROM)	Can user programs or operating system write data to it during normal operation?	Purpose? (e.g. boot code)	How is data input to this memory?	How is this memory write protected?	How is the memory cleared?
Secondary MCU	Non-volatile	1	IC703	64KB	Internal Flash	No	Boot code, FW	The data is flash via Dell Update Package (DUP)	SW write protected	Before firmware update, the memory will be cleared.
FRU	Non-volatile	1	IC601	16KB	EEPROM	No	PSU information	During Manufacturing, by programming the image via firmware update process	SW write protected	User cannot clear the memory.
ARTESYN PSU										
Primary MCU	Non-volatile	1	U317	64KB	Internal Flash	No	Boot code, FW	The data is flash via Dell Update Package(DUP)	SW write protected	Before firmware update, the memory will be cleared.
Secondary MCU	Non-volatile	1	U301	32KB	Internal Flash	No	Boot code, FW	The data is flash via Dell Update Package(DUP)	SW write protected	Before firmware update, the memory will be cleared.
FRU	Non-volatile	1	U315	128KB	Internal Flash	No	DC controller FW and FRU data	During Manufacturin	SW write protected	User cannot clear the memory.

Item	Non-Volatile or Volatile	Quantity	Reference Designator	Size	Type (e.g. Flash PROM, EEPROM)	Can user programs or operating system write data to it during normal operation?	Purpose? (e.g. boot code)	How is data input to this memory?	How is this memory write protected?	How is the memory cleared?
								g, by programming the image via firmware update process		
LiteOn PSU										
Primary MCU	Non-volatile	1	IC050	64K	Internal Flash	No	Boot code, FW	The data is flash via Dell Update Package (DUP)	SW write protected	Before firmware update, the memory will be cleared.
Secondary MCU/FRU	Non-volatile	1	IC900	128K	Internal Flash	No	Boot code, FW	The data is flash via Dell Update Package (DUP)	SW write protected	Before firmware update, the memory will be cleared.
R1B										
MCU	Non-volatile	1	U1	8kB	Flash ROM	No	Riser information	The data is flash via iDRAC auto update	No write protected. Not visible to Host Processor	User cannot clear the memory.
R2A										
MCU	Non-volatile	1	U1	8kB	Flash ROM	No	Riser information	The data is flash via	No write protected. Not	User cannot clear the memory.

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								iDRAC auto update	visible to Host Processor	
R2B										
MCU	Non-volatile	1	U1	8kB	Flash ROM	No	Riser information	The data is flash via iDRAC auto update	No write protected. Not visible to Host Processor	User cannot clear the memory.
R3A										
MCU	Non-volatile	1	U1	8kB	Flash ROM	No	Riser information	The data is flash via iDRAC auto update	No write protected. Not visible to Host Processor	User cannot clear the memory.
R3B										
MCU	Non-volatile	1	U1	8kB	Flash ROM	No	Riser information	The data is flash via iDRAC auto update	No write protected. Not visible to Host Processor	User cannot clear the memory.

NOTE: For any information that you may need, direct your questions to your Dell Marketing contact.

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