Statement of Volatility – Dell EMC PowerEdge XE7100, XE7420, XE7440

Dell EMC PowerEdge XE7100, XE7420, XE7440 contains both volatile and non-volatile (NV) components. Volatile components lose their data immediately upon removal of power from the component. Non-volatile components continue to retain their data even after the power has been removed from the component. Components chosen as user-definable configuration options (those not soldered to the motherboard) are not included in the Statement of Volatility.
Configuration option information (pertinent to options such as microprocessors, remote access controllers , and storage controllers) is available by component separately. The following NV components are present in the PowerEdge XE7100, XE7420, XE7440 server.

Item	Non-Volatile or Volatile	Quantity	Reference Designator	Size
SAS EXPANDER BAORD				
NVSRAM Memory	Non-Volatile	1	U4	1MB
BP FRU (SELF PORT)	Non-Volatile	1	U6	2KB
BP FRU (OTHER PORT)	Non-Volatile	1	U7	2KB
EXP FRU	Non-Volatile	1	U8	2KB
Configure-Zoning	Non-Volatile	1	U9	128KB
FLASH	Non-Volatile	1	U_FLASH_S1	128MB
2.5” SSD BP				
SEP internal flash	Non-Volatile	1	U5	Flash:64KB EEPROM:2KB
MID-Plane				
FRU	Non-Volatile	1	U9	2KB
FH Riser Board				
CR_SPI	Non-Volatile	1	U2	512K Bytes
MBC_RGT_CP	Non-Volatile	1	U3	32M bit
X16 CABLE MAIN RISER BOARD				
CR_SPI	Non-Volatile	1	U7	512K Bytes
MBC_RGT_CP	Non-Volatile	1	U5	32M bit
X16 Riser board				
CR_SPI	Non-Volatile	1	U2	512K Bytes
MBC_RGT_CP	Non-Volatile	1	U1	32M bit

Item	Non-Volatile or Volatile	Quantity	Reference Designator	Size
PCIE Switch board(Gen4)				
EEROM	Non-Volatile	1	U14	128M bit
FRU	Non-Volatile	1	U15	128K bit
3.5” HDD BP				
FRU	Non-Volatile	1	U97	2KB
CPLD A	Non-Volatile	1	U83	4K (LE)
CPLD B	Non-Volatile	1	U73	4K (LE)
MB Bridge Board				
FRU	Non-Volatile	1	U2	2KB
Power Delivery Board (PDB)				
Microcontroller	Non-Volatile	1	U23 (NXP)	Up to 1MB
FRU	Non-Volatile	1	U30	256Kbit
Flash	Non-Volatile	1	U10	16Mbit
FPGA	Non-Volatile	1	U25	1,88Mbit
Rover MB				
PCH Internal CMOS RAM	Non-Volatile	1	U_LBG	256 Bytes
BIOS Password (part of PCH internal CMOS RAM)	Non-Volatile	1	U_LBG	16 Bytes (out of 256 Bytes used for PCH Internal CMOS RAM)
Primary BIOS SPI Flash	Non-Volatile	1	U_SPI_BIOS	32 MB
iDRAC SPI Flash	Non-Volatile	1	U_BMC_SPI1	4 MB
BMC eMMC	Non-Volatile	1	U_EMMC	4 GB
CPU Vcore and Memory regulator	Non-Volatile	2	PU2, PU9	16 KB
Vmem Regulators	Non-Volatile	2	PU15, PU21	16 KB
System CPLD RAM	Volatile	1	U_CPLD	92 KB
System CPLD FLASH	Non-Volatile	1	U_CPLD	256 KB
System Memory: RDIMM and LRDIMM	Volatile	Up to 16 per CPU	CPU1<2:1>_CH<5:0>_D<1:0>	Up to 64 GB per DIMM
System Memory: NVDIMMM-N	Non-Volatile	Up to 4 per CPUs 1 and 2 (12 total in system)	CPU1<2:1> _CH<5:0>_ D1	128 GB per NVDIMMN

Internal USB Key	Non- Volatile	Up to 1	INTERNAL_USB1	Varies (not factory installed)
CPU	Volatile	1 or 2	CPU1 / CPU2	Various
iDRAC DDR	Volatile	1	U_IDRAC9_DRAM1	512 MB
iDRAC	Volatile	1	U_IDRAC	For CPU:128 KB + registers Co-proc: 64 Kb + registers
PIROM	Non-Volatile	1 or 2	CPU1 / CPU2	256 Bytes
Recovery BIOS SPI	Non-Volatile	1	U_REC_SPI_BIOS	16 MB

Item	Type (e.g. Flash PROM, EEPROM)	Can user programs or operating system write data to it during normal operation?	Purpose? (e.g. boot code)
SAS EXPANDER BOARD			
NVSRAM Memory	NVSRAM	NO	Configuration data
BP FRU (SELF PORT)	FRU	NO	BP manufacturing information
BP FRU (OTHER PORT)	FRU	NO	BP manufacturing information
EXP FRU	FRU	NO	Board manufacturing information
Zoning-Configure FRU	FRU	NO	HDD zoning configure information
FLASH	Flash	YES	PM8056 firmware
2.5” SSD BP			
SEP internal flash	Flash	No	FW configuration data
MID-Plane			
FRU	FRU	No	Board manufacturing information
FH Riser Board			
CR_SPI	Flash PROM and EEPROM	No	Card reader configuration Settings FW
MBC_RGT_CP	Flash PROM and EEPROM	Yes	
X16 CABLE MAIN RISER BOARD			
CR_SPI	Flash PROM and EEPROM	No	Card reader configuration Settings FW
MBC_RGT_CP	Flash PROM and EEPROM	Yes	
X16 Riser board			
CR_SPI	Flash PROM and EEPROM	No	Card reader configuration Settings FW
MBC_RGT_CP	Flash PROM and EEPROM	Yes	
PCIE Switch board(Gen4)			
EEROM	Flash PROM and EEPROM	No	Broadcom PEX88080 configuration Settings FW
FRU	Flash PROM and EEPROM	No	FRU
3.5” HDD BP			
FRU	FRU	No	Board manufacturing information
CPLD A	CPLD	Yes	Enable HDD online & fault LED, collect HSC fault event and report to CM, cable detect function

Item	Type (e.g. Flash PROM, EEPROM)	Can user programs or operating system write data to it during normal operation?	Purpose? (e.g. boot code)
CPLD B	CPLD	Yes	Enable HDD online & fault LED, collect HSC fault event and report to CM, cable detect function.
MB bridge board			
FRU	FRU	No	Board manufacturing information.
Power Delivery Board (PDB)			
Microcontroller	include up to 1 MB of flash	NO (For normal customer/user ,there is no way can go to the customer and update him)	Report PSU and Chassis Management (MCU + FPGA) control firmware.
FRU	FRU	NO (For normal customer/user ,there is no way can go to the customer and update him)	PDB PPID information
Flash	Flash	NO (For normal customer/user ,there is no way can go to the customer and update him)	Chassis Management (FPGA FW) control firmware.
FPGA	FPGA	NO (For normal customer/user ,there is no way can go to the customer and update him)	Enable Chassis Management (FPGA FW) control firmware.
Rover MB			
PCH Internal CMOS RAM	Battery-backed CMOS RAM	No	Real-time clock and BIOS configuration settings.
BIOS Password (part of PCH internal CMOS RAM)	Batterybacked CMOS RAM	Yes	Password to change BIOS settings.
Primary BIOS SPI Flash	SPI Flash	No	Boot code.
iDRAC SPI Flash	SPI Flash	No	iDRAC Uboot (bootloader)
BMC eMMC	eMMC NAND Flash	No	Operational iDRAC FW, Lifecycle controller (LC) USC partition, LC service diags, LC OS drivers, USC firmware.
CPU Vcore and Memory regulator	ROM	No	Operational parameters
Vmem Regulators	ROM	No	Operational parameters
System CPLD RAM	Flash	No	Not utilized

Item	Type (e.g. Flash PROM, EEPROM)	Can user programs or operating system write data to it during normal operation?	Purpose? (e.g. boot code)
System CPLD FLASH	RAM	No	Power on System firmware
System Memory: RDIMM and LRDIMM	DRAM	Yes	System OS RAM
System Memory: NVDIMMM-N	Flash -NVDIMM	No	Data integrity
Internal USB Key	Flash	Yes	General purpose USB key drive
CPU	Cache + registers	Yes	Processor cache + registers
iDRAC DDR	DRAM	No	iDRAC local memory
iDRAC	Cache + registers	No	Processor cache + registers
PIROM	EEPROM	No	Processor info + scratchpad
Recovery BIOS SPI	SPI Flash	No	Recovery image

Item	How is data input to this memory?	How is this memory write protected?	How is the memory cleared?
SAS EXPANDER BOARD			
NVSRAM Memory	PM8056 writes configuration data to NVSRAM	Not WP. Not visible to Host Processor	User cannot clear the memory.
BP FRU (SELF PORT)	Pre-programmed before assembly	Not WP	The user cannot clear memory.
BP FRU (OTHER PORT)	Pre-programmed before assembly	Not WP	The user cannot clear memory.
EXP FRU	Pre-programmed before assembly	Not WP	The user cannot clear memory.
Zoning-Configure FRU	PM8056 writes zoning data to FRU	Not WP	The user cannot clear memory.
FLASH	Pre-programmed before assembly	Not WP	The user cannot clear memory.
2.5" SSD BP			
SEP internal flash	Pre-programmed before assembly	Not WP	The user cannot clear memory.
MID-Plane			
FRU	Programmed at ICT during production.	Not WP	The user cannot clear memory.
FH Riser Board			
CR_SPI	Pre-programmed before assembly.	Not WP	
MBC_RGT_CP	SPI interface via iDRAC	Software write protected	
X16 CABLE MAIN RISER BOARD			
CR_SPI	Pre-programmed before assembly.	Not WP	
MBC_RGT_CP	SPI interface via iDRAC	Software write protected	
X16 Riser board			
CR_SPI	Pre-programmed before assembly.	Not WP	
MBC_RGT_CP	SPI interface via iDRAC	Software write protected	
PCIE Switch board(Gen4)			
EEROM	Pre-programmed before assembly	Not WP.	Cannot be cleared with existing tools available to the customer.
FRU	Programmed at ICT during production.	Not WP	Cannot be cleared with existing tools available to the customer.

Item	How is data input to this memory?	How is this memory write protected?	How is the memory cleared?
3.5" HDD BP			
FRU	Pre-programmed before assembly.	Not WP.	User cannot clear the memory.
CPLD A	Pre-programmed before assembly or PM8056 flash CPLD FW by I2C bus.	Not WP.	Use expander DUP to update PM8056 & CPLD FW.
CPLD B	Pre-programmed before assembly or PM8056 flash CPLD FW by I2C bus.	Not WP.	Use expander DUP to update PM8056 & CPLD FW.
MB bridge board			
FRU	Pre-programmed before assembly.	Not WP.	User cannot clear the memory.
Power Delivery Board (PDB)			
Microcontroller	Pre-programmed before assembly. Can be updated using pass through by CM(JTAG/UART) tools	Not WP. Not visible to Host Processor	Cannot be cleared with existing tools available to the customer
FRU	Programmed at BFT during production.	Not WP.	Cannot be cleared with existing tools available to the customer
Flash	Pre-programmed before assembly. On-Line: It can be updated using pass through by CM(JTAG/UART) tools. Off-Line: It can be updated using pass through by EEPROM copy machine tools	Not WP. Not visible to Host Processor	Cannot be cleared with existing tools available to the customer
FPGA	Pre-programmed before assembly. Can be updated using pass through by CM(JTAG/UART) tools	Not WP. Not visible to Host Processor	Cannot be cleared with existing tools available to the customer
Rover MB			
PCH Internal CMOS RAM	BIOS	N/A - BIOS only control	Perform the following steps: 1) Set NVRAM_CLR jumper to clear BIOS configuration settings at boot and reboot system. 2) AC power off system, remove coin cell battery for 30 seconds, replace battery and power on. 3) Restore default configuration in F2 system setup menu.
BIOS Password (part of PCH internal CMOS RAM)	Keyboard	N/A - BIOS only control	1) Place shunt on J_PSWD_NVRAM jumper pins 2 and 4. 2) AC power off is required after placing the shunt. 3) AC power on with the shunt in place and then can be removed.

Item	Type (e.g. Flash PROM, EEPROM)	Can user programs or operating system write data to it during normal operation?	Purpose? (e.g. boot code)
Primary BIOS SPI Flash	SPI Interface via PCH	Software write protected	Not possible with any utilities or applications and system is not functional if corrupted/removed.
iDRAC SPI Flash	SPI interface via iDRAC	Embedded iDRAC Subsystem firmware actively controls sub area based write protection as needed.	User cannot clear completely. However, user data, lifecycle log and archive, SEL, fw image repository can be cleared via delete configuration and retire system, accessible in Lifecycle controller interface.
BMC eMMC	NAND Flash interface via iDRAC	Embedded FW write protected	User cannot clear completely. However, user data, lifecycle log and archive, SEL, fw image repository can be cleared via delete configuration and retire system accessible in Lifecycle controller interface.
CPU Vcore and Memory regulator	Programmed at factory via I2C	No write protect	User cannot clear.
Vmem Regulators	Programmed at factory via I2C	no write protect	User cannot clear.
System CPLD RAM	Not utilized	Not accessible	Not accessible.
System CPLD FLASH	Firmware update	BIOS Security Protocols	User cannot clear.
System Memory: RDIMM and LRDIMM	System OS	OS Control	Reboot or power down system.
System Memory: NVDIMMM-N	When system initiates a Save (AC loss, shutdown, etc.) NVDIMM-N controller will transfer data from DRAM to Flash.	Neither system nor OS can access the flash, only a system initiated Save will trigger the NVDIMM-N controller to transfer data from DRAM to flash.	Using BIOS menu option, select NVDIMM factory reset.
Internal USB Key	USB interface via PCH. Accessed via system OS	No write protect	Can be cleared in system OS.
CPU	Various	Various	Remove A/C.
iDRAC DDR	iDRAC Firmware	No write protect	Remove A/C.
iDRAC	iDRAC Firmware	No write protect	Remove A/C.
PIROM	SMBus interface to iDRAC	128 bytes protected by Intel/128 bytes not protected	User cannot clear.
Recovery BIOS SPI	SPI interface via iDRAC	No write protect	User cannot clear.

NOTE: For any information that you may need, direct your questions to your Dell Marketing contact.