Statement of Volatility – Dell EMC DSS8440

The Statement of Volatility provides you information related to volatile and non-volatile components of different configurations of Dell EMC DSS servers.

Volatile components lose their data when the system is powered off and disconnected from the electrical outlet, whereas, non-volatile components continue to retain their data even when the system is powered off.

The following table provides information of the different configurations of the DELL EMC DSS8440 server.

Item	Non-Volatile or Volatile	Quantity	Reference Designator	Size
PSB				
PCIe SW	Non-volatile	4	PESW_SPI1~PESW_SPI4	128MB
FRU	Non-volatile	1	U16	128Kb
CPLD - Embedded Block RAM	Volatile	1	U2002	92Kb
CPLD- User FLASH Memory	Non-volatile			96Kb
CPLD- CFG. FLASH Memory	Non-volatile			720Kb
MCU	Non-volatile	4	U10~U13	16KB
PDB				
CPLD - Embedded Block RAM	Volatile	1	U_CPLD1	92Kb
CPLD- User FLASH Memory	Non-volatile			96Kb
CPLD- CFG. FLASH Memory	Non-volatile			720Kb
10x2.5” Backplane				
SEP	Non-volatile	1	U_SEP1	Flash:64KB+4KB EEPROM: 2KB
Planer				
PCH Internal CMOS RAM	Non-Volatile	1	U_PCH	256 Bytes
BIOS SPI Flash	Non-Volatile	1	U212(PRIM_SPI_BIOS)	32 MB
iDRAC SPI Flash	Non-Volatile	1	U217(UBOOT)	4 MB
BMC EMMC	Non-Volatile	1	U_EMMC1	8 GB
System CPLD RAM	Volatile	1	U_CPLD1	92 KB

Item	Non-Volatile or Volatile	Quantity	Reference Designator	Size
System Memory	Volatile	Up to 12 per CPU	CPU<2:1>_CH<5:0>_D<1:0>	Up to 32GB per DIMM
Power Supplies				
PSU FW	Non-Volatile	1 per PSU	Varies by part number	64K for each DSP (Primary and Secondary)

Item	Type (e.g. Flash PROM, EEPROM)	Can user programs or operating system write data to it during normal operation?	Purpose? (e.g. boot code)
PSB			
PCIe SW	FLASH	Yes	PCIe switch FW
FRU	FRU	No	Manufacturing information
CPLD - Embedded Block RAM	RAM	No	Not utilized
CPLD- User FLASH Memory	FLASH	No	Not utilized
CPLD- CFG. FLASH Memory	FLASH	Yes	System information
MCU	MCU	No	NVMe hot plug feature
PDB			
CPLD - Embedded Block RAM	RAM	No	Not utilized
CPLD- User FLASH Memory	FLASH	No	Not utilized
CPLD- CFG. FLASH Memory	FLASH	Yes	Power on system
10x2.5" Backplane			
SEP	Integrated Flash+EEPROM	No	HDDBP Firmware + FRU
Planer			
PCH Internal CMOS RAM	Battery-backed CMOS RAM	No	Real-time clock and BIOS configuration settings
BIOS SPI Flash	SPI Flash	No	Boot code, system configuration information, UEFI environment, Flash Descriptor, ME
iDRAC SPI Flash	SPI Flash	No	iDRAC Uboot (bootloader), server management persistent store (i.e. IDRAC MAC

Item	Type (e.g. Flash PROM, EEPROM)	Can user programs or operating system write data to it during normal operation?	Purpose? (e.g. boot code)
			Address, iDRAC boot variables), lifecycle log cache, virtual planar FRU and EPPID, rac log, System Event Log, JobStore, iDRAC Secure boot code,
BMC EMMC	eMMC NAND Flash	No	Operational iDRAC FW, Lifecycle Controller (LC) USC partition, LC service diags, LC OS drivers, USC firmware
CPU Vcore and VSA Regulators	OTP(one time programmable)	No	Operational parameters
System CPLD RAM	RAM	No	Not utilized
System Memory	RAM	Yes	System OS RAM
Power Supplies			
PSU FW	Embedded microcontroller flash	No	Power Supply operation, power management data and fault behaviors

Item	How is data input to this memory?	How is this memory write protected?
PSB		
PCIe SW	Offline programming by factory	No write protect
FRU	Programmed at ICT during production	No write protect
CPLD - Embedded Block RAM	Not utilized	Not accessible
CPLD- User FLASH Memory	Not utilized	Not accessible
CPLD- CFG. FLASH Memory	Firmware update	Not accessible
MCU	Offline programming by factory	No write protect
PDB		
CPLD - Embedded Block RAM	Not utilized	Not accessible
CPLD- User FLASH Memory	Not utilized	Not accessible
CPLD- CFG. FLASH Memory	Firmware update	Not accessible
10x2.5" Backplane		

Item	How is data input to this memory?	How is this memory write protected?
SEP	Offline programming by factory	NA
Planer		
PCH Internal CMOS RAM	BIOS	N/A – BIOS only control
BIOS SPI Flash	SPI interface via PCH	Software write protected
iDRAC SPI Flash	SPI interface via iDRAC	Embedded iDRAC subsystem firmware actively controls sub area based write protection as needed.
BMC EMMC	NAND Flash interface via iDRAC	Embedded FW write protected
CPU Vcore and VSA Regulators	Programmed at factory via I2C	No write protect
System CPLD RAM	Not utilized	Not accessible
System Memory	System OS	OS control
Power Supplies		
PSU FW	Different vendors have different utilities and tools to load the data to memory. It can also be loaded by Dell Update Package from LC or OS (Windows and Linux)	Protected by the embedded microcontroller. Special keys are used by special vendor provided utilities to unlock the ROM with various CRC checks during load.

NOTE: For any information that you may need, direct your questions to your Dell Marketing contact.